Si9136: Novel Triple-Converter Controller

by Kin Shum

INTRODUCTION

The Si9136 is the industry's first triple-converter controller designed for notebook computer main power bus applications. Two high-efficiency, high-power buck converters take the input power from the battery or the ac power supply and create 3.3-V and 5-V outputs. The third converter is a two-switch buck-boost topology that generates a 12-V output from a wide range of input voltages.

Key functions of the Si9136 controller are discussed in the "Description of Operation" section of the data sheet. In this application note, additional descriptive information is provided and design guidelines are given for both buck and buck-boost configurations. These are followed by demo board test results demonstrating device efficiency at various operating voltages. For more general buck converter design guidelines, please review Siliconix application notes AN715 and AN710.

IC DESCRIPTION

The Si9136 is a BiCMOS controller that offers five possible dc output voltages. Three power outputs, namely 5 V, 3.3 V, and 12 V, can be controlled by the pins provided by the IC. One low-power 5-V output (V_L pin), capable of handling a load up to 30 mA, is available whenever the input is powered from 5.5 V_{DC} to 30 V_{DC}. One precision 3.3-V output becomes available if any one or more of the three power outputs is activated, and it is capable of supplying loads up to 1 mA. Note that the 5-V V_L output is active regardless of whether the power outputs are activated.

The Si9136 controller is packaged in the TSSOP-28. A functional block diagram of the IC's internal structure is shown in Figure 1, 2, and 3.

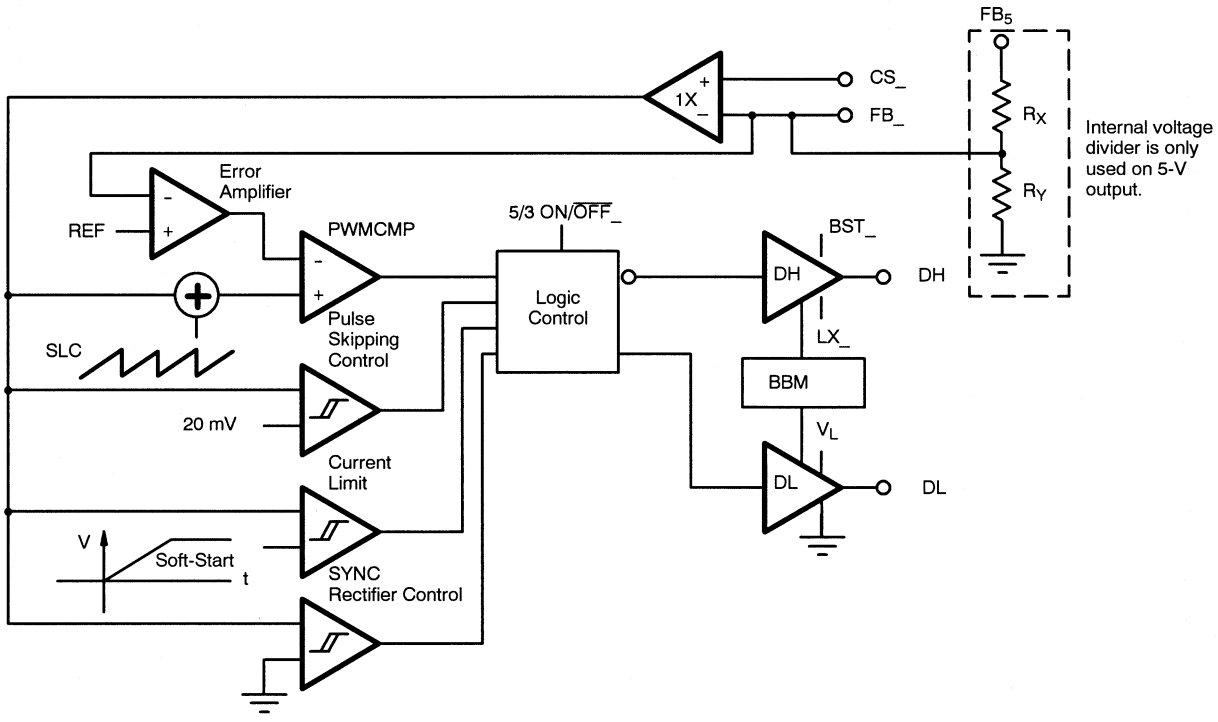

FIGURE 1. Buck Block Diagram

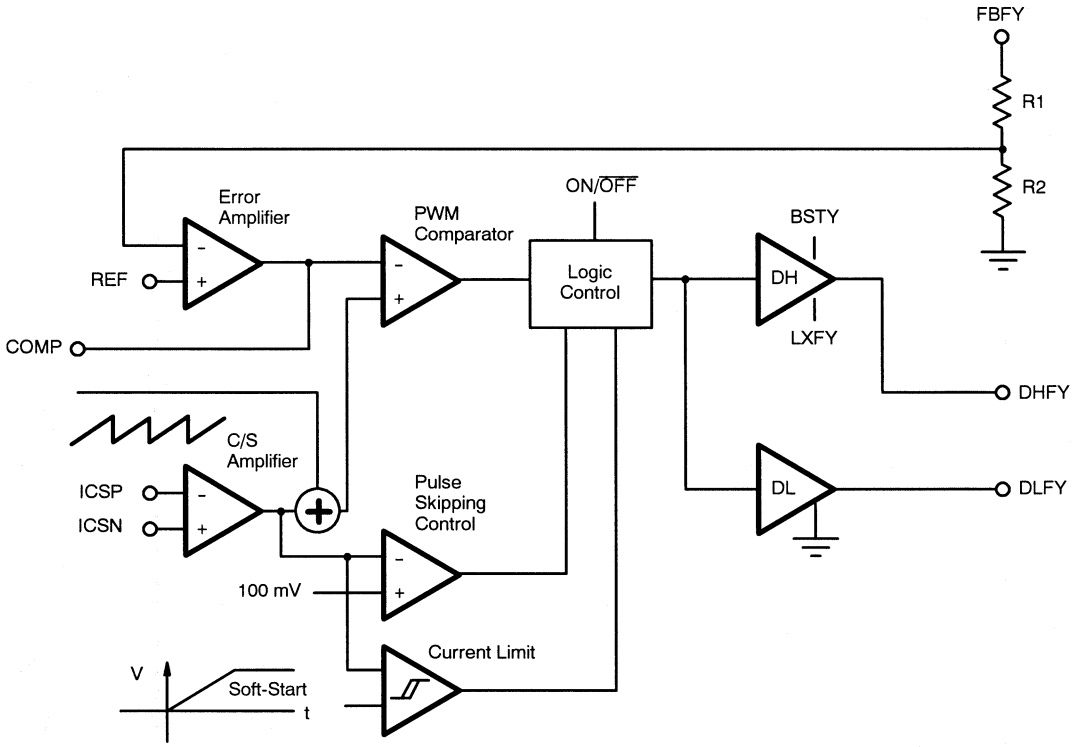

FIGURE 2. PWM Flyback Block Diagram

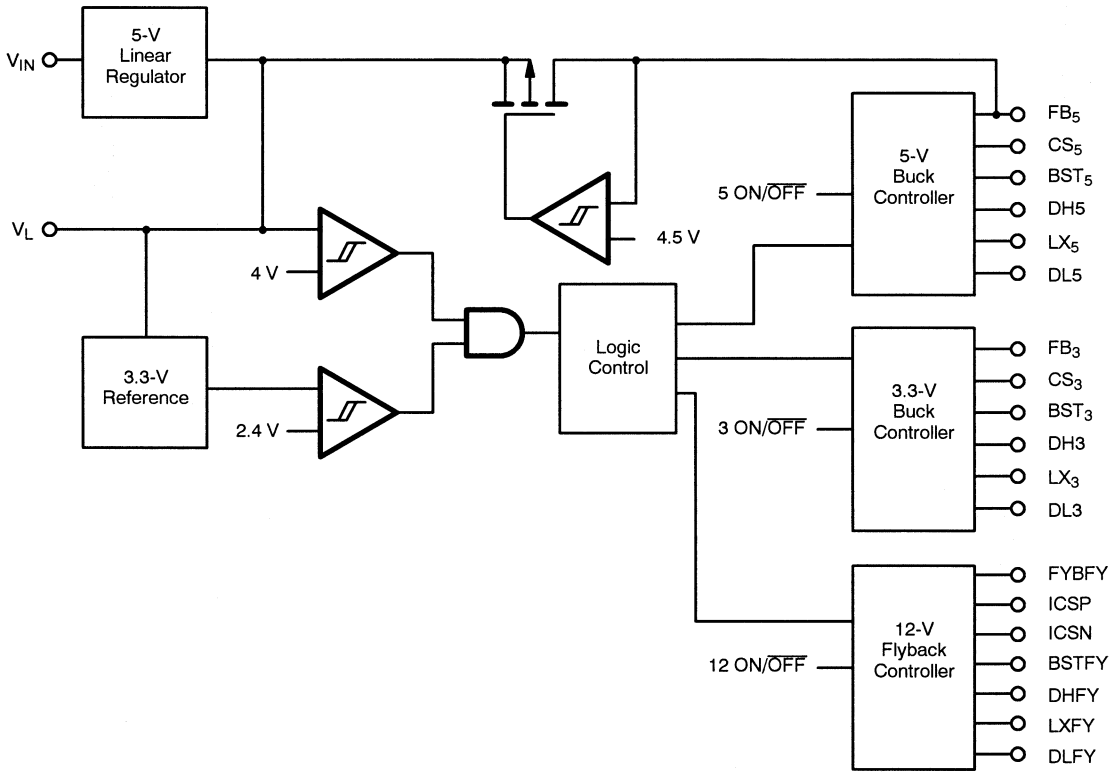

FIGURE 3. Complete Si9136 Block Diagram

Start-Up

With an input voltage over 5.5 V, the internal linear regulator of the Si9136 can instantly produce 5 V at its V_L pin. A soft-start feature is built in for all three switching converters individually.

When a converter is turned on, the peak inductor current is controlled to rise gradually over the soft-start time, typically 4 ms, to avoid excessive inrush current and voltage overshoots at the output.

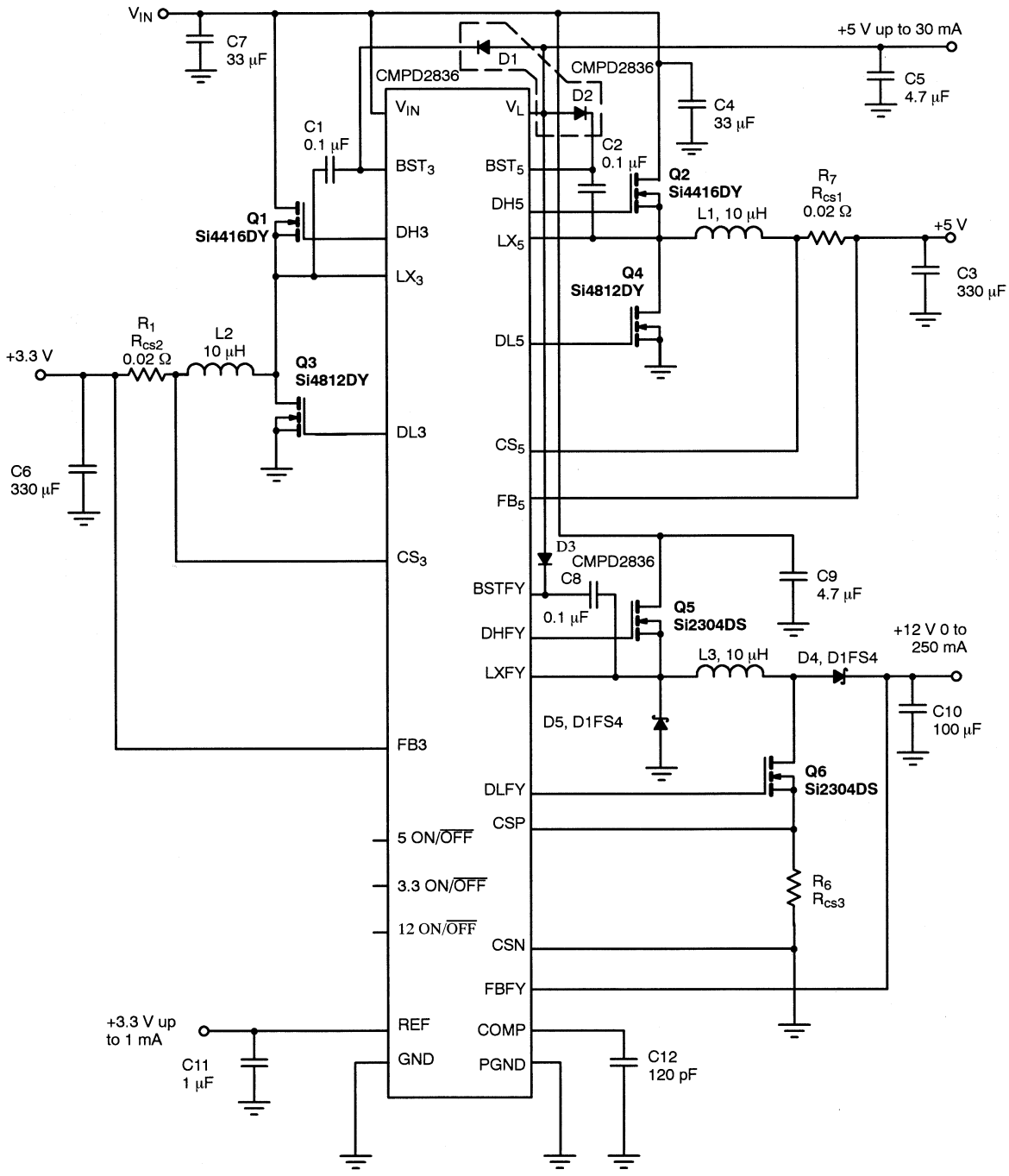

FIGURE 4. Typical Application Circuit

Converter Configuration

All three converters in the Si9136 are constant-frequency, pulse-width modulation (PWM) or pulse skipping modulation (PSM) current-mode controlled switching regulators. The switching frequency is fixed at 200 kHz inside the IC for all three converters. A typical application circuit is shown in Figure 4. The 3.3-V and 5-V converters are synchronous buck (or step-down) converters, because the input voltage is always higher than the output. Both MOSFET gate drive signals from the controller, DH and DL, are designed for n-channel power MOSFETs. The upper rail for the low-side driver (DL) is 5 V and can drive the MOSFET directly. Since the high-side switch is floating, the logic high for the driver has to be referenced to the logic low (LX). When the high-side switch is on, the LX pin voltage level is the same as V_{IN}. So V_{GS} needs to be built on top of the LX. A flying capacitor (C1 or C2) is connected between the upper rail of the high-side driver (BST) and LX. V_L replenishes this capacitor to one diode drop below 5 V through D1 or D2 when the low-side switch is on.

The 12-V converter is a two-switch, two-diode buck-boost, or a non-isolated flyback topology. The conversion ratio of this buck-boost converter in continuous conduction mode (CCM) is

$$V_O = V_{IN}\frac{D}{1-D} + 2V_D \quad (1)$$

Where V_D is the forward drop of each diode, which is normally neglected for ease of analysis thanks to the low forward drop of Schottky diodes. Since the factor D/(1 - D) can be either below or above 1, the converter can either step up or step down the input voltage. For lower power levels (e.g. a maximum of 250 mA in the application circuit), it is desirable to operate the buck-boost converter in discontinuous-continuous mode (DCM). Please see “Inductor Selection,” for more details. The duty ratio in DCM, given below, is different from that in CCM:

$$D = \frac{1}{V_{IN}}\sqrt{\frac{2V_O I_{OUT} L}{T_S}} \quad (2)$$

Where TS is the switching period. However, the converter is still able in DCM to step up and step down the input voltage. Note that the duty cycle in DCM is also a function of the load, I_{OUT}.

Figure 5 illustrates the duty cycles required to keep outputs regulated throughout the input voltage range for all three converters. The curves show buck-boost converter operation with 100-mA and 250-mA loads.

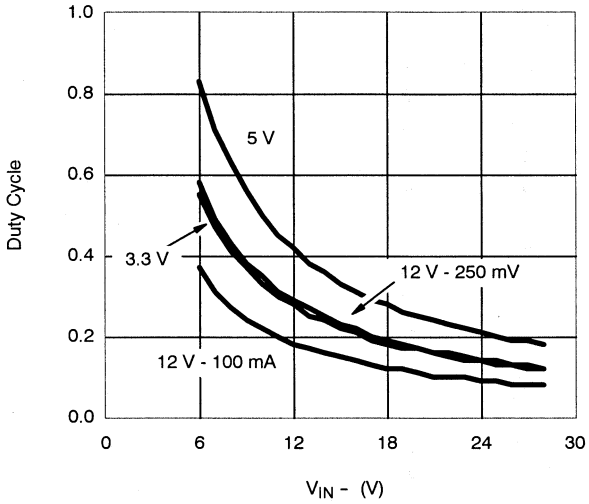

FIGURE 5. Switching Duty Cycle for All Converters vs. V_{IN}

DESIGN GUIDELINES

The Si9136 combines a high level of device integration with room for design flexibility. Key components required for a complete converter design are power MOSFETs, current sensing resistors, inductors, and input/output capacitors.

MOSFET/Diode Selection

Next to choosing the controller IC, the second most important component of a converter design is selecting the right switching component. Today MOSFETs serve this function in most converter circuits. The key parameters of a MOSFET are its drain-to-source voltage rating, drain current rating, gate-to-source voltage rating, on-resistance, total gate charge (Q_g), switching speed, and package. To choose the proper parameters, one has to understand the operating conditions of the circuit.

Parameter/Selection Criteria

- Voltage Rating: Input voltage except the low side switch of the buck-boost converter, which only sees output 12 V plus a diode drop
- Current rating: Input current except the low side switches of the buck converters, which carry the differential current between output and the input.
- Gate-to-Source Voltage: The maximum rating should be above 5 V (provided by most power MOSFETs)
- On-Resistance and Gate Charge: An optimum combination of the two is critical to achieving high-efficiency operation
- Switching Speed: Faster speeds minimize crossover switching losses, so select MOSFETs with short t_r, t_f, $t_{d(on)}$, and $t_{d(off)}$ times. The higher of the two sums $t_r + t_{d(on)}$ and $t_f + t_{d(off)}$, has to be less than 30 ns, which is the minimum break-before-make (BBM) time.
- Package: The package must be capable of dissipating power adequately while also meeting size requirements

A key concern is balancing on-resistance and gate charge. Formerly this was a difficult task, since in typical MOSFETs, low on-resistance is accompanied by an increase in gate charges losses in high-frequency switching applications. For both 3.3-V and 5-V buck converters, Siliconix's PWM-optimized power MOSFETs solve this problem. The Si4416DY is recommended for the high side switch, and the Si4812DY for the low-side switch. Both devices offer high efficiency with maximum loads from 4 A to 8 A. The Si2304DY in the SOT-23 is a perfect choice for the 12-V converter for both high and low side switches, with maximum load ratings from 150 mA to 250 mA.

A critical issue in synchronous converters is shoot-through. During switch-on and switch-off transitions, the rise and fall times of the MOSFETs, together with the delay time, create a momentary period where both switches are on. For a synchronous buck converter, this forms a short circuit path for the input voltage, and current can shoot through both switches to ground instantaneously. Shoot-through can seriously deteriorate efficiency, and in extreme cases can destroy the switches. The Si9136's output drive signals feature a BBM time of 30 ns minimum, allowing clean transitions between switches. During the BBM time, the inductor current flows through the diode in parallel with the low-side MOSFET. To avoid the conduction of the MOSFET body diode, Siliconix recommends connecting an external Schottky diode across the low-side MOSFET. The Si4812DY is specially designed for synchronous converter applications with an integrated Schottky diode.

Inductor Selection

An inductor is the energy storage component in a converter. Choosing an inductor means specifying its size, structure, material, inductance, saturation level, dc-resistance (DCR), core loss, and other characteristics. Fortunately, there are many inductor vendors that offer wide selections with ample specifications and test data, such as Vishay Dale, Coilcraft, Coiltronics, and Sumida. Following are some key parameters that users should focus on.

In PWM mode, inductance has a direct impact on the ripple current. The peak-to-peak inductor ripple current for a buck converter can be calculated as

$$I_{p-p} = \frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN}Lf} \quad (3)$$

Where f is the switching frequency.

Higher inductance means a lower ripple current, lower rms current, lower voltage ripple on both input and output, and higher efficiency. However, higher inductance also means a larger inductor size, higher series resistance, and slower response to transients. It is common to design this I_{p-p} to be about 30% of the dc current level for a synchronous buck converter. For this application, Siliconix recommends a 10-µH inductor, which results in 1.29-A and 1.67-A p-p current levels with a 15-V input voltage for 3.3-V and 5-V converters, respectively. See Figure 6 for various input voltage levels.

Inductance has a similar effect on buck-boost converter designs. However, there is a different design goal involved, which is to force the converter operating in DCM to avoid the right-hand-plane (RHP) zero. This control issue will be discussed later. The inductance has to be below a certain value for DCM operation, and this critical level varies with input voltage:

$$L_{CRIT} = \frac{V_{OUT}V_{IN}^2}{2(V_{OUT} + V_{IN})^2 I_{OUT} f} \quad (4)$$

Where I_{OUT} is the maximum load current.

Figure 7 shows the dividing curve between CCM and DCM with maximum load of 250 mA over the input range. The curve explains the choice of a 10-µH inductor for the application circuit. In DCM, the peak inductor current can be calculated as

$$I_{PK} = \sqrt{\frac{2V_O I_{OUT} T_S}{L}} \quad (5)$$

Note that this peak current is a function of the load but not of the input voltage, as illustrated in Figure 6.

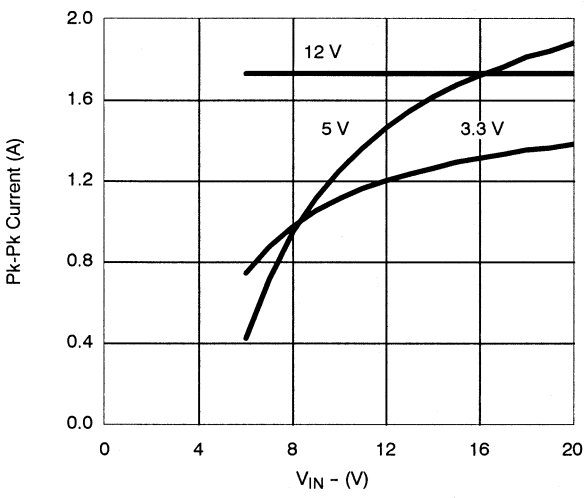

FIGURE 6. Peak-to-Peak Inductor Current for the Application Circuit

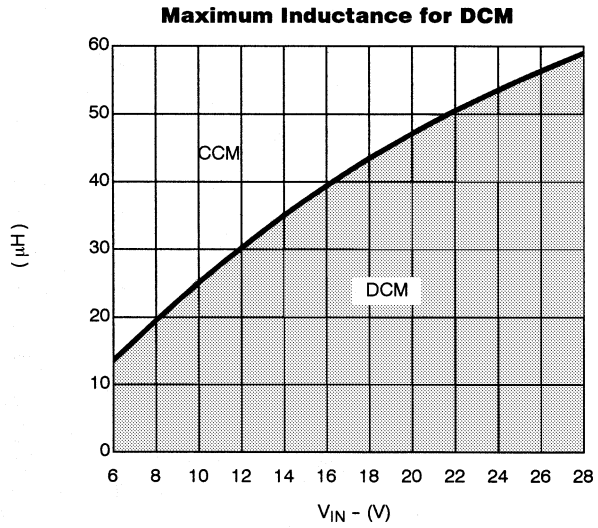

FIGURE 7. Buck-Boost Critical Inductance with 250-mA Maximum Load

The saturation level is another important parameter in choosing inductors. Note that the saturation currents specified in data sheets are maximum ratings. For a dc-dc converter operating in PWM mode, this maximum current is the peak inductor current. The peak current for a buck converter can be calculated using (6), while for a buck-boost converter it has already been derived in (5).

$$I_{PK} = I_{OUT} + \frac{I_{p-p}}{2} \quad (6)$$

This peak current varies with inductance tolerance and other factors, and the rated saturation level varies over temperature. A sufficient design margin is thus required when choosing current ratings.

A high-frequency core material, such as ferrite, should be chosen to reduce core loss. The DCR should be kept as low as possible to reduce conduction loss.

The inductance also has an effect on the current limit and PSM threshold point. Please refer to next section for more details.

Sense Resistor

The Si9136 is a current-mode controller, and current sensing resistors are used to sense the inductor current, or to switch current in the case of the buck-boost circuit, for accurate control. The resistor determines the converter current limit and the transition current level between PWM and PSM operation.

The current sense signal is compared with a current limit reference voltage V_{CL}, which is typically 125 mV for the 3.3-V and 5-V converters and 410 mV for the 12-V converter. When the sense signal exceeds V_{CL}, the converter reaches the current limit and the output voltage starts to sag. The sensing resistance value required for certain systems can be easily calculated as

$$R_{CS} = \frac{V_{CL}}{I_{PK}} \quad (7)$$

while I_{pk} can be substituted from (5) or (6). Using a 20-mΩ RCS as shown in the application circuit, the current limits of both buck converters are plotted over the input range in Figure 8.

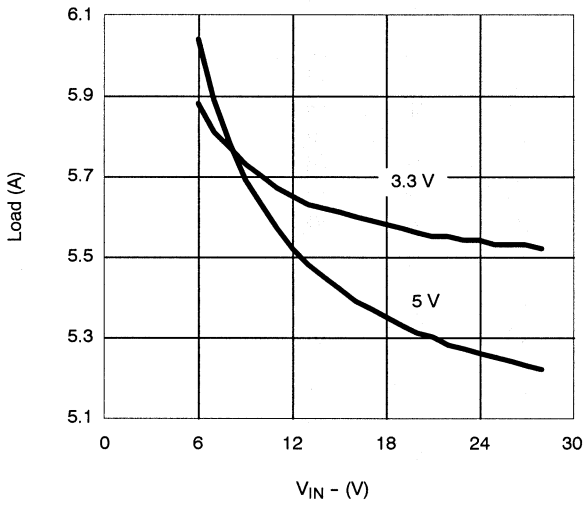

FIGURE 8. Buck Converter Current Limit with R_{CS} = 20 mΩ

In the case of the buck-boost converter, choosing the resistor is slightly more complicated, since it is desirable to operate in DCM. The sensing resistor has to be low enough for the converter to deliver maximum load before hitting the current limit, and it also has to be high enough to limit the current before the converter runs into CCM. The critical load separating DCM and CCM is plotted in Figure 9. Also shown in the same plot is the current limit with a 200-mΩ sensing resistor, which is below the critical load line to ensure DCM operation.

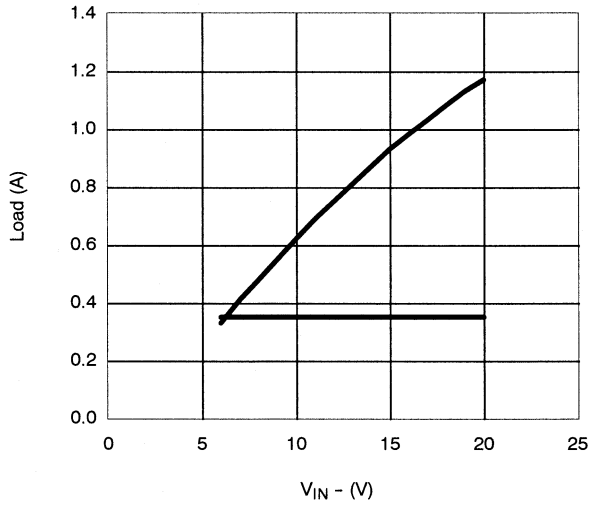

FIGURE 9. Buck-Boost Critical Load and Current Limit

The current sensing signal is also compared with a minimum peak reference voltage V_{MP}, which is typically 20 mV for the 3.3-V and 5-V converters and 100 mV for the 12-V converter. When the sensing signal drops to V_{MP}, the converter starts to skip pulses while maintaining the peak current at V_{MP}/R_{CS}.

For the application circuit, where R_{CS} is 20 mΩ, the critical load for the buck converter triggering the transition between PWM and PSM at various input levels is plotted in Figure 10. This critical load for the buck-boost converter with a 200-mΩ sensing resistor is a constant 21 mA over the full input range.

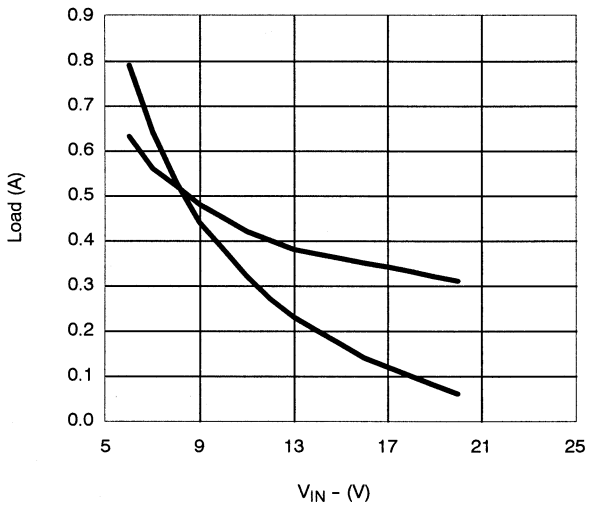

FIGURE 10. Buck Critical Load Separating PWN and PSM

Input/Output Capacitor Selection

Low-ESR (effective series resistance) capacitors are required on both the input and the output to minimize voltage ripple. Both tantalum and Sanyo OSCON type capacitors offer low ESR as well as high capacitance density. The capacitance and the ESR of the output capacitor also affect the loop stability. For buck converters, the minimum capacitance and the maximum ESR required to ensure stability are given in (8) and (9).

$$C_{OUT} \geq \frac{V_{REF}}{2\pi V_{OUT} R_{CS} BW} \quad (8)$$

$$ESR \leq \frac{V_{OUT} R_{CS}}{V_{REF}} \quad (9)$$

Where V_{REF} is 3.3 V, and BW is the control loop bandwidth of 50-kHz typical. For the buck-boost converter, the output capacitance has a big effect on the output voltage ripple. A 100-µF tantalum cap is used in the application circuit and the output voltage ripple is slightly under 100 mV with a 250-mA load. Note that the ripple is directly proportional to the load. If lower ripple is required, a small, second-stage L-C filter, rated at 1 µH and 10 µF, works perfectly.

Stability

In PWM operation, the converters run with a fixed switching frequency and current-mode control. The peak inductor current is regulated by the error voltage of the voltage regulation amplifier. The current control loop is called the inner loop, while the voltage control loop is called the outer loop. The transconductance nature of the inner control loop reduces the effect of the inductor on the output L-C filter. This makes it easier to stabilize the control loop since the output filter becomes a first-order R-C instead of a complex, second order R-L-C. Despite its good features, current-mode control does not affect the power stage right half plane (RHP) zero in all boost-derived topologies, including buck-boost converters. This RHP zero can cause problems for certain converters since it is a duty cycle and load-dependent zero that increases the loop gain while dropping the phase. When it occurs close to the loop gain crossover frequency, the loop can easily break into oscillation due to an insufficient phase margin or no phase margin at all. Fortunately this RHP zero does not exist if the converter operates in DCM, so it is desirable for the 12-V buck-boost converter to run in DCM.

Layout Issues

One of very few drawbacks of switching power supplies is the noise level induced from their high frequency switching operation. However, the noise level can be minimized by properly laying out the components. Here are some tips for laying out the converters with Si9136 controller.

- A multilayer board is preferred. Use the top layer for high-power traces and parts, the bottom layer for low-power, noise-sensitive traces and parts, and the inner layer as ground plane.
- Minimize the length of heavy current traces, and keep the trace at least 5 mm wide. The high current ground trace should be kept as short as possible.
- Minimize the trace length of current sensing. Use a Kelvin connection (Figure 11) to avoid any error caused by load current.
- Place the inductor and the switching node (LX, DH, DL, BST) away from the sensitive analog signals (CS, FB, REF, V_L) to reduce noise coupling.
- Decoupling caps for V_L and REF have to be right next to the pin.
- Use a separate ground for low-power control circuitry (signal ground), including the REF cap, “GND” pin, and COMP (Si9136 only). Connect the signal ground-to-power ground at a single point, preferably at the PGND pin.

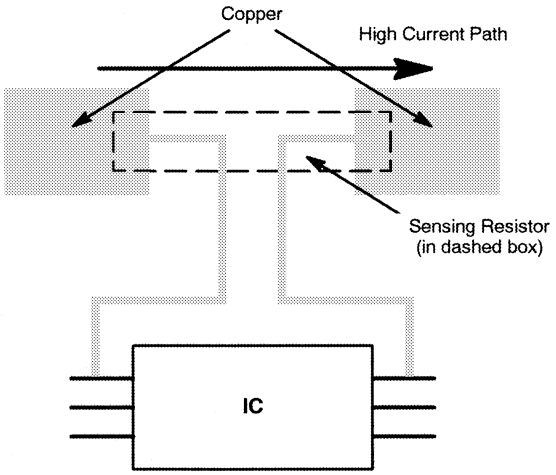

FIGURE 11. Sensing Resistor Kelvin Connection

Other Issues

The level shifting capacitor for gate drives C1, C2 and C8 should be large enough to drive the MOSFETs. The required capacitance increases with the size of the MOSFET, because of gate charge, since the capacitor has to be large enough to maintain certain voltage level while discharging to drive the MOSFET. Normally a 0.1-µF capacitor should be enough to drive any MOSFET with a gate charge of 50 nC or less.

EXPERIMENTAL RESULTS

The Si9136 controller has been fully tested in both buck and boost modes on demo boards. Some efficiency results are plotted here. Please refer to the Si9136 data sheet for more waveforms.

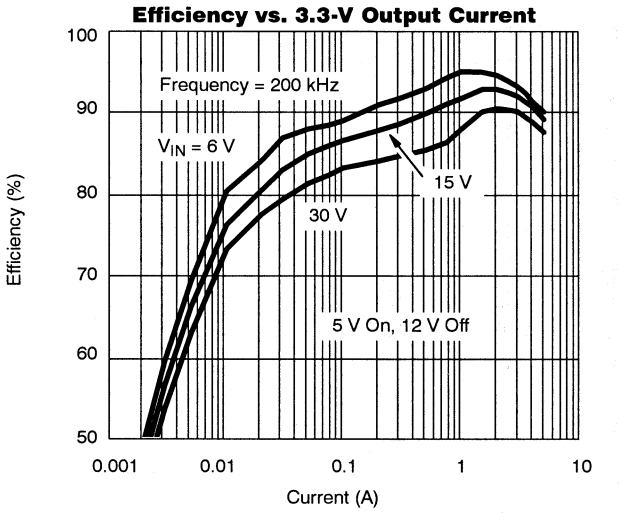

FIGURE 12. 3.3-V Converter Efficiency

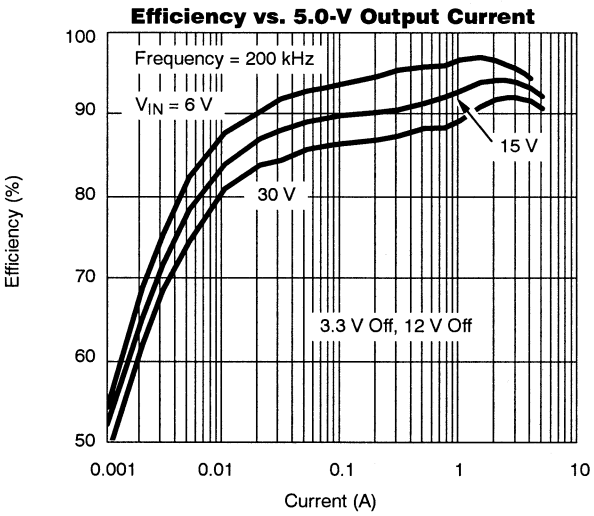

FIGURE 13. 5-V Converter Efficiency

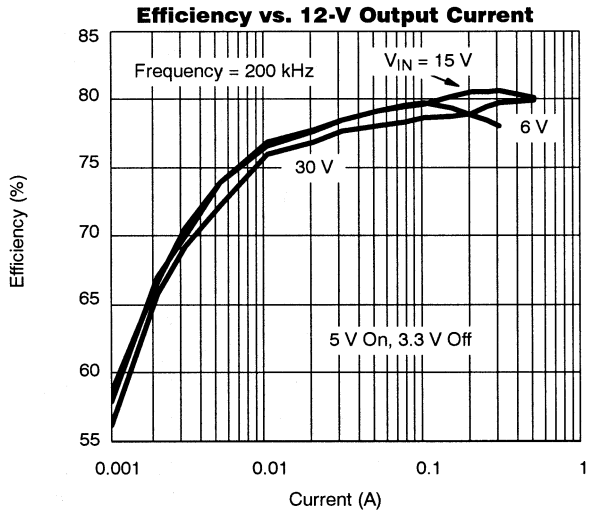

FIGURE 14. 12-V Converter Efficiency